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				Application Number		New Application	
				Filing Date		December 16, 2003	
				First Named Inventor		Etsuko ASANO et al.	
				Art Unit			
Examiner				Attorney Docket Number		740756-2688	
Sheet	1	of	1				

U.S. PATENT DOCUMENTS					
Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	U.S. Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			

FOREIGN PATENT DOCUMENTS						
Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>3</sup>
		Country Code <sup>4</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
REP		JP 08-139044	05/31/1996	Otani		Abstract

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
REP		Mitsumasa KOYANAGI, "SUBMICRON DEVICE II", Maruzen Kabushiki Kaisha Shuppan, 1987, pp. 121-142.	
REP		Masahide INUISHI et al., "A HIGH PERFORMANCE AND HIGHLY RELIABLE DUAL GATE CMOS WITH GATE/N OVERLAPPED LDD APPLICABLE TO THE CRYOGENIC OPERATION", IEDM, 1989, pp. 773-776.	
REP		Takashi HORI, "1/4-μm LATID (LArge-Tilt-angle Implanted Drain) TECHNOLOGY FOR 3.3-V OPERATION", IEDM 1989, pp. 777-780.	

Examiner Signature		Date Considered	1/20/06
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